

AMENDMENTS TO THE CLAIMS

1. (currently amended) A wafer bonding method to form integrated chips, comprising:

selectively depositing a plurality of metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of adjacent wafers;

depositing at least a barrier line on an outer edge of each of the opposing surfaces of the adjacent wafers;

selectively aligning the adjacent wafers to form a stack; and

~~bonding the metallic lines and the barrier line on the surface of one wafer with the metallic lines and the barrier line on the surface of the other wafer to establish electrical connections between active IC devices on adjacent wafers and to form a barrier structure on the outer edge of the adjacent wafers.~~

bonding exposed portions of the metallic lines on the opposing surfaces of the adjacent wafers to establish electrical connections between active integrated circuit (IC) devices on the adjacent wafers; and

bonding the barrier lines on the opposing surfaces of the adjacent wafers to form a barrier structure on the outer edge of the adjacent wafers.

2. (currently amended) The wafer bonding method as claimed in claim 1, wherein the metallic lines are Copper (Cu) bonding pads ~~deposited on opposing surfaces of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.~~

3. (currently amended) The wafer bonding method as claimed in claim 1, wherein the metallic lines are surrounded by a dielectric recess ~~to ensure that the metallic lines deposited on the surface of one wafer are bonded with the metallic lines deposited on the surface of the other wafer.~~

4. (original) The wafer bonding method as claimed in claim 1, wherein the bonded

wafers includes a plurality of individual die and the barrier structure is formed on the outer edge of the bonded wafers to protect internal die from corrosion, contamination and crack propagation when the bonded wafers are cut into individual die.

5. (original) The wafer bonding method as claimed in claim 4, wherein the barrier structure is a dense grid of connected copper (Cu) lines in a checkerboard pattern erected on the outer edge of usable die.

6. (original) The wafer bonding method as claimed in claim 5, wherein the barrier structure is erected on the outer edge of usable die using an edge reticle.

7. (currently amended) The wafer bonding method as claimed in claim 1, wherein the bonded wafers correspond to a single die and the barrier structure is formed by one or more barrier lines deposited on the outer edge of the ~~bonded~~ single die to protect the ~~bonded~~ single die from corrosion, contamination and crack propagation.

8. (currently amended) The wafer bonding method as claimed in claim 7, wherein the barrier lines correspond to concentric copper (Cu) guard rings deposited on the perimeter of the ~~bonded~~ single die to serve as passivation barriers.

9. (currently amended) A method of forming a three-dimensional (3-D) integrated chip system, comprising:

forming a first wafer ~~including~~ to include one or more integrated circuit (IC) devices, a first set of metallic lines deposited ~~via an~~ into a first interlevel dielectric (ILD) on a surface of the first wafer, and ~~at least one~~ a first barrier line deposited on an outer edge of the surface of the first wafer; and

forming a second wafer ~~including~~ to include one or more integrated circuit (IC) devices, a second set of metallic lines deposited ~~via an~~ into a second interlevel dielectric (ILD) on a surface of the second wafer, and ~~at least one~~ a second barrier line deposited on an outer edge of the surface of the second wafer,

~~wherein the metallic lines and the barrier line deposited on the surface of the second wafer are bonded with the metallic lines and the barrier line deposited on the~~

~~surface of the first wafer to establish electrical connections between active IC devices on adjacent wafers and to form a barrier structure on the outer edge of the adjacent wafers.~~

bonding exposed portions of the first set of metallic lines to exposed portions of the second set of metallic lines to establish electrical connections between active IC devices on the first and second wafers; and

bonding the first barrier line to the second barrier line to form a barrier structure on the outer edge of the first and second wafers.

10. (currently amended) The method as claimed in claim 9, wherein the sets of metallic lines include Copper (Cu) bonding pads ~~deposited on opposing surfaces of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.~~

11. (original) The method as claimed in claim 9, wherein the bonded wafers includes a plurality of individual die and the barrier structure is formed to protect internal die from corrosion, contamination and crack propagation when the bonded wafers are cut into individual die.

12. (original) The method as claimed in claim 11, wherein the barrier structure is a dense grid of connected copper (Cu) lines in a checkerboard pattern erected on the outer edge of usable die.

13. (original) The method as claimed in claim 12, wherein the barrier structure is erected on the outer edge of usable die using an edge reticle.

14. (currently amended) The method as claimed in claim 9, wherein the bonded wafers correspond to a single die and the barrier structure is formed by one or more barrier lines deposited on the outer edge of the ~~bonded~~ single die to protect the ~~bonded~~ single die from corrosion, contamination and crack propagation.

15. (currently amended) The method as claimed in claim 14, wherein the barrier lines correspond to concentric copper (Cu) guard rings deposited on the perimeter of

the ~~bonded~~ single die to serve as passivation barriers.

16. (currently amended) A method of forming a three-dimensional (3-D) integrated chip system, comprising:

forming a first wafer ~~including~~ to include one or more active integrated circuit (IC) devices;

forming a second wafer ~~including~~ to include one or more active integrated circuit (IC) devices;

depositing first metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of the first and second wafers at designated locations to serve as wafer bonding pads and to establish electrical connections between active IC devices on the first and second wafers, when the first and second wafers are bonded; and

depositing second metallic lines on an outer edge of opposing surfaces of the first and second wafers to form a barrier structure, when the first and second wafers are bonded.

17. (currently amended) The method as claimed in claim 16, wherein the first metallic lines include a plurality of Copper (Cu) bonding pads ~~deposited on opposing surfaces of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.~~

18. (currently amended) The method as claimed in claim 16, wherein the second metallic lines include a plurality of Copper (Cu) barrier lines deposited on the outer edge of the adjacent first and second wafers to protect active IC devices from corrosion and contamination.

19. (currently amended) The method as claimed in claim 16, wherein the barrier structure is a dense grid of connected copper (Cu) lines in a checkerboard pattern erected on the outer edge of usable die within the bonded wafers.

20. (original) The method as claimed in claim 19, wherein the barrier structure is erected on the outer edge of usable die using an edge reticle.

21. (currently amended) The method as claimed in claim 16, wherein the bonded wafers correspond to a single die and the barrier structure is formed to protect the ~~bonded~~ single die from corrosion, contamination and crack propagation.

22. (currently amended) The method as claimed in claim 21, wherein the second metallic lines correspond to concentric copper (Cu) guard rings deposited on the perimeter of the ~~bonded~~ single die to serve as passivation barriers.

23. (new) A method comprising:

selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers, wherein the adjacent wafers include a first and second wafer and the plurality of metallic lines are surrounded by a dielectric recess to ensure that the metallic lines on the first wafer contact the metallic lines on the second wafer;

selectively aligning the adjacent wafers to form a stack; and

bonding the metallic lines on the opposing surfaces of the adjacent wafers to electrically connect active integrated circuit (IC) devices on the adjacent wafers.

24. (new) A method comprising:

depositing a first barrier line on an outer edge of a surface of a first wafer having a plurality of die;

depositing a second barrier line on an outer edge of a surface of a second wafer having a plurality of die; and

bonding the first and second barrier lines to bond the first and second wafers and to form a barrier structure on the outer edge of the bonded wafer.

25. (new) A method comprising:

depositing a first set of concentric guard rings on a perimeter of a first die;

depositing a second set of concentric guard rings on a perimeter of a second die;

and

bonding the first and second set of concentric guard rings to bond the first and second die and to form a barrier structure on the perimeter of the bonded die.